REMARKS/ARGUMENTS

This is a submission accompanying an RCE and serves as a response to the Advisory Action issued May 31, 2006, (hereinafter referred to as "the Advisory Action"), and the Final Office Action of January 10, 2006, (hereinafter referred to as "the Final Office Action"), in connection with the above-identified application and elaborates on and adds to the Request for Reconsideration mailed to the Patent Office on April 10, 2006. Reconsideration of the application is respectfully requested.

In the Final Office Action, claims 1-3 and 5-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hu et al., U.S. Patent Application Publication US2003/0157773A1, in view of Wolf and Tauber, Silicon Processing for the VLSI Era Volume I: Process Technology. Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hu et al. in the Final Office Action. Reconsideration of the rejections is respectfully requested.

It is respectfully submitted that the Examiner's finding in the Advisory Action is incorrect. The Examiner alleged therein that "it is Hu that establishes an RTP for oxidation at 1100C and not Wolf and thus it, according to Wolf, be the highest temperature of the semiconductor-making process," (Advisory Action, page 2, lines 4-5) The Examiner is, however, respectfully requested to identify where Hu et al. teaches establishing an RTP for oxidation at 1100C. What Hu et al. teaches is only that "RTO process conditions may include a temperature generally in the range of 700C to 1100C (for example, 100C)," (paragraph [0025], lines 6-8). Here, the value of 100C is out of the range of 700C to 1000C and is not meaningful at all. Even if "100 C" is nothing more than a typographical error and thus Hu et al.'s intention is "1000C," Hu et al. merely teaches one example in his intended range of 700C to 1100C. Thus, Hu et al. at most teaches the temperature range (700C to 1100C) of RTO with one example to achieve the purpose of his disclosure. More importantly, Hu et al. merely discusses the concentration of nitrogen in the gate insulating film, and does not at all concern heat treatments such as impurity activation, which are carried out later than RTO.

Turning to Wolf and Tauber, it discloses unwanted dopant diffusion being caused by processes in VLSI fabrication being carried out at sufficiently high temperatures, 900C, (page

57), and teaches carrying out RTP for impurity activation in the range of 420-1150C, (page 58, lines 14-15, 24). Thus, Wolf and Tauber merely discusses impurity diffusion/activation and does not at all involve RTO, which is carried out earlier than impurity diffusion/activation to form gate insulating film. More importantly, although Wolf and Tauber teaches the unwanted diffusion being caused by temperatures at or above 900C, Wolf and Tauber teaches 420-1150C as the temperature of RTP.

Therefore, the combination of Hu et al. and Wolf and Tauber results in a process wherein RTO is carried out in the temperature range of 700-1100C for gate insulating film, and then RTP is carried out in the temperature range of 420-1150C for impurity activation. It is, thus, respectfully submitted that the combination of Hu et al. and Wolf and Tauber neither teaches nor suggests an explicit relationship in magnitude between RTO temperature and RTP temperature. The temperature for RTO may be lower than the temperature for RTP even if RTO is carried out at the highest temperature in the range specified, 1100C. Furthermore, even if the impurity activation is carried out at such a temperature that does not cause unwanted dopant diffusion, as discussed in Wolf and Tauber (that is, lower than 900C), the RTO may be carried out at a temperature that is in a range of 700-900C, in accordance with the teaching of Hu et al.

In contrast, one of the features as defined in claims 1-12, 22, and 23 is in the relationship in magnitude between RTO temperature and RTP temperature. That relationship is that the RTO temperature is higher than the RTP temperature, and that relationship is neither taught nor suggested by Hu et al. and Wolf and Tauber, taken alone or in combination. More importantly, the Examiner is respectfully requested to take note of the fact that the problems to be solved by the present invention have been discovered by the inventor himself, and have not been discussed or addressed by any one of Hu et al. and Wolf and Tauber. As explained above, Hu et al. merely discusses RTO, and Wolf and Tauber merely discloses RTP used in processes such as impurity activation, and any one of them does not disclose that a gate insulating film subjected to RTO may be damaged by RTP that is carried out after RTO.

New claims 22 and 23, directly or indirectly dependent upon claim 1, have been added to clarify the scope of coverage of independent claim 1. Antecedent basis for new claim 22 is

found in the specification, for example, on page 17, lines 25-26. Antecedent basis for new claim 23 is found in the specification, for example, on page 21, lines 13-18.

Independent claim 13 has been amended to provide, in part, for, "[a] semiconductor device comprising: ... an oxide film formed on the semiconductor substrate and having a first surface on a side of said semiconductor substrate and a second surface on an opposite side to said semiconductor substrate, ... wherein the nitrogen in the oxide film has, in a direction of a depth in the oxide film, a concentration profile that monotonically increases from the second surface of the oxide film toward the first surface of the oxide film to reach a peak value and then monotonically decreases up to the first surface of the oxide film ...." Antecedent basis for the amendments to independent claim 13 is found in the specification, for example, on page 17, lines 1-4; page 19, lines 9-17; and page 20, lines 2-3, and in the drawings, for example, in Figs. 5(b), 6(a), and 6(b).

The Examiner, in the Advisory Action, alleges that, "[r]egarding claims 13 and 21, Hu's figure 6 describes the same process as that of Applicant. The percentage of nitrogen would decrease in an exponential manner as it goes deeper into the oxide, however, the concentration of nitrogen would decrease in a constant manner," (page 2, lines 5-7).

Fig. 6 illustrates oxygen and nitrogen concentrations in a dielectric layer 20 which has a thickness of 22 Å, (paragraphs [0029] - [0030]), and Fig. 6 also shows nitrogen and oxygen concentrations in a semiconductor substrate 11, (Fig. 5; paragraph [0019]), since Fig. 6 covers a depth of 60 Å, beyond the 22 Å of depth of dielectric layer 20. It is plain from an examination of the graph that double peaks are shown for the nitrogen concentration with a relatively flat area between the double peaks.

In contrast, independent claim 13 requires monotonically increasing nitrogen concentration from the surface of the oxide film opposite to the semiconductor substrate towards the first surface of the oxide film on the semiconductor substrate to reach a peak value and then monotonically decreasing nitrogen concentration to the first surface of the oxide film.

Since claims 14-20 are directly or indirectly dependent upon independent claim 13, the remarks above with respect to independent claim 13 apply equally to claims 14-20.

Independent claim 21 has a feature of the nitrogen in the second portion of the gate oxide film being free from substantial distribution into the gate electrode. The Examiner points out, with regard to claim 20, (Office Action, page 4, paragraph 14), that Hu et al. discloses nitrogen being free from substantial distribution into the gate electrode, (paragraph [0026]), but there is no description about the gate electrode in the paragraph. In paragraph [0026], the last sentence discloses that the dielectric layer 20 has a relatively uniform nitrogen profile resulting from the nitridation and oxidation processes, leading to a slower defect generation rate through dielectric layer 20. This sentence only discloses how to form the gate dielectric layer. Because there is no description of gate electrode formation and other processes after gate formation, the nitrogen distribution into the gate electrode after thermal treatment at a higher temperature than the RTO process is not known.

In view of the foregoing amendments and remarks, allowance of claims 1-23 is respectfully requested.

Accordingly, the Examiner is respectfully requested to reconsider the application, allow the claims and pass this case to issue.

Respectfully submitted,

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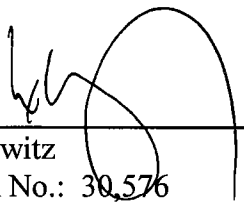

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